IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

A. MORGENSHTEIN et al

Serial No.:

oplicant:

10/648,474

Filed:

August 27, 2003

For:

Logic Circuit and Method of

Logic Circuit Design

Examiner:

Group Art Unit: 2819

Attorney

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888888

Docket: 26327

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a PTO Form 1449 which lists citations which may be material to the patentability and examination of the above identified application. Also enclosed are copies of the references cited. These are submitted in compliance with the duty of disclosure defined in 37 CFR 1.56. The Examiner is requested to make these citations of official record in this application.

This Information Disclosure Statement under 37 CFR 1.56 is not to be construed as a representation that a search has been made, that additional matter which is material to the examination of this application does not exist, or that any or more of these citations constitutes prior art.

Respectfully submitted,

Registration No. 25,457

Date: March 30, 2004

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Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.									
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